22. (Amended) The semiconductor device of Claim 6, wherein said sidewall offset in said at least one of said drain and source diffusion layers extends only towards one of said source and drain diffusion layers, the other of said at least one of said drain and source diffusion layers having no sidewall offset.

REMARKS

This paper is being provided in response to the September 13, 2001 Final Office Action for the above-referenced application. In this response, applicant has amended claims 1, 6 and 22 in order to more particularly point out and distinctly claim that which applicant deems to be the invention. Applicant respectfully submits that the amendments to the claims are supported by the originally filed specification.

In response to the objection to claims 6 and 22, applicant has amended claims 6 and 22 to clarify that the independent claim recites at least one sidewall, and that the dependent claim discloses a feature for the only one side wall case. Applicant believes that this amendment clarifies the meaning of the claims, and is fully responsive to the objection set forth in the Office Action. Accordingly, applicant respectfully requests that this objection be withdrawn.

The rejection of claims 1, 5-6, 11, 20 and 22 under 35 U.S.C. 102(b) as being anticipated by Gonzales (U.S. Patent No. 5,39, 835, hereinafter referred to as "Gonzales") is hereby traversed and reconsideration thereof is respectfully requested. Applicant

respectfully submits that claims1, 5-6, 11, 20 and 22, as amended herein, are neither disclosed nor suggested by Gonzales.

Applicant's claim 1, as amended herein, recites a semiconductor device having a substrate, and an insulating film formed at a surface of the substrate for defining device regions in each of which a semiconductor device is to be fabricated. There is a gate electrode formed on the substrate, and at least one sidewall covers the gate electrode. There are drain and source diffusion layers formed at a surface of the substrate around the gate electrode. The sidewall has a sidewall offset extending outwardly of the gate electrode along a surface of the substrate in at least one region below which the drain and source diffusion layers are formed. The sidewall offset extends along a surface of a gate oxide film on which the gate electrode is formed. At least one of the drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset by an amount greater than the depth of the source and drain diffusion in a vertical direction. Claim 5 depends from claim 1.

Applicant's claim 6, as amended herein, recites a semiconductor device having a semiconductor substrate, an insulating film formed at a surface of the substrate defining device regions in each of which a semiconductor device is to be fabricated. There is a gate electrode formed on the substrate, and at least one sidewall covering the gate electrode. The drain and source diffusion layers are formed at a surface of the substrate around the gate electrode. The sidewall has at least one sidewall offset extending outwardly of the gate electrode along a surface of the semiconductor substrate in the

regions below which the drain and source diffusion layers are formed. The sidewall offset extends along a surface of a gate oxide film on which the gate electrode is formed. There are also low-resistive wiring layers formed at surfaces of the drain and source diffusion layers. The low-resistive wiring layers are located outwardly beyond a peripheral edge of the sidewall offset. At least one of the drain and source diffusion layers extending towards the gate electrode beyond an edge of the sidewall offset by an amount greater than the depth of the source and drain diffusion in a vertical direction. Claims 11, 20 and 22 depend from claim 6. Claim 22 recites that the sidewall offset in said at least one of said drain and source diffusion layers extends only towards one of the source and drain diffusion layers. The other of the drain and source diffusion layers having no sidewall offset.

The cited reference of Gonzales discloses a process for fabricating a CMOS dynamic random access memory. This process uses a high energy ion implantation of boron ions that is performed at a oblique angle for punch through protection. Figure 9, and the associated portions of the specification, disclose metal 92 connected to the graded junction 24B formed by the oblique implantation. The metal 92 is remote from peripheral edge of the sidewall offset. There are also disclosed metal lines 51 that are directly upon the sidewall film.

Applicant respectfully submits that amended claims 1 and 6 have features not disclosed by the cited reference of Gonzales, specifically "*...drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset by an*

amount greater than a depth of said source and drain diffusion in a vertical direction ...", as recited in independent claims 1 and 6. The cited reference discloses a diffusion 23 that is aligned by reference to the sidewall oxide film 21, and a diffusion 71 aligned to the oxide film 41, and thus neither diffusion can possibly extend under the alignment oxide by as much as the depth of the diffusion, as a matter of simple physics. By contrast the present application discloses a double diffused drain layer 63 that has at least one component of the diffusion that is aligned to an edge of the oxide 53 that extends horizontally over the region of the first diffusion. This is discussed in more detail in the present specification at least starting at page 11, line 4. Further, the disclosed device does not have the metal lines 51 situated such that "*...said low-resistive wiring layers being located outwardly beyond a peripheral edge of said sidewall offset ...*", as recited in independent claim 6. As noted above, the metal lines are in direct contact with the sidewall film, and thus this feature is not found in the cited reference.

Accordingly, at least the above described two features of the present application's independent claims are not found, disclosed nor suggested by the cited reference, and thus the independent claims, and the corresponding dependent claims that contain further patentable features over the base claim, can not be anticipated by the cited reference. Accordingly, applicant respectfully requests that this rejection be withdrawn.

The rejection of claims 3-4, 6, 9-10 and 22 under 35 U.S.C. 103(a) as being unpatentable over Gonzales in view of Cheng is hereby traversed and reconsideration

thereof is respectfully requested. Applicant respectfully submits that claims 1-11 are neither disclosed nor suggested by the references taken separately or in combination.

The features of the cited reference of Gonzales are discussed above. The features of the independent claims are also discussed above. The features of the cited reference of Cheng include an insulated gate semiconductor device having gate electrodes, and including source region 57 and drain region 58, source region 59 and drain region 62. Openings in a layer of dielectric material 63, expose portions of the S/D regions 57, 58, 59, and 62, and portions 28 and 29 of gate electrodes 35 and 35'. Silicide 64 is formed on the exposed S/D regions 57, 58, 59, and 62 and on the exposed portions of 35 and 35'. An insulating layer 66 is formed on layers 63 and 64. Openings formed in the layer 66 expose portions of layer 64. Dopant regions 57 and 58 are formed having a concentration ranging from $1x10^{19}$ atoms/cm^3 to approximately $5x10^{20}$ atoms/cm^3. Dopant regions 43 and 44 have concentrations ranging between $1x10^{16}$ to $5x10^{17}$ atoms/cm^3.

Applicant's amended independent claim 1, from which claims 3-4 depend, is neither described nor suggested by the suggested combination of Cheng with Gonzales, since neither reference discloses nor suggests the combination of features of "... *a semiconductor device that includes a sidewall offset extending along a surface of a gate oxide film on which the gate electrode is formed ....*", or "*...drain and source diffusion layers extending towards said gate electrode beyond an edge of said sidewall offset by an amount greater than a depth of said source and drain diffusion in a vertical direction ...*" as set forth in applicant's amended claim 1.

Cheng discloses an insulating layer 66 formed on a layer of dielectric material and silicide 64, but neither describes nor suggests a sidewall offset that extends along a surface of a gate oxide film, nor does Cheng describe or suggest that the S/D diffusions extend in the fashion discussed above with reference to the 102 rejection, as found in applicant's amended claim 1.

Applicant's claim 6 is also neither disclosed nor suggested by Cheng for reasons similar to those set forth regarding amended claim 1. Therefore, since the independent claims are not obvious over the suggested combination of cited references, then the dependent claims 3-4, 6 9-10 and 22, which contain further patentable features over the base claim, also can not be rendered obvious by the suggested combination of cited references. Applicant respectfully requests that this rejection, as set forth in the Office Action, be withdrawn.

The rejection of claim 7 under 35 U.S.C. 103(a) as being unpatentable over Gonzales in view of Cheng, and further in view of Kunishima, is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claim 7 is neither disclosed nor suggested by the suggested combination of cited references, whether taken separately or in any combination.

The features and disclosure of Gonzales and Cheng are discussed above, as are the features of the independent claims of the present application. The cited reference of

Kunishima discloses a semiconductor device such as an FET. There is an SiO2 film 23 and a BPSG film 25 sequentially deposited on top of a substrate that is lamp annealed to increase the concentration of the p+ type impurity diffusion layer 17, as shown in Figure 5C. There is also a $TiSi_2$ layer 21 shown in Figure 5C, and discussed at column 10, lines 16-59. Figure 5A shows a gate oxide film 5 and a gate electrode having stacked films, which is discussed at column 9, lines 32-35. Dependent claim 7, which depends from claim 6, recites that the low resistive wiring layers are composed of TiSi.

Applicant respectfully submits that the cited reference of Kunishima adds nothing significant to the other cited references in that Kunishima also neither discloses nor suggests a semiconductor device that includes a sidewall offset extending along a surface of a gate oxide film on which the gate electrode is formed, as set forth in applicant's amended claim 6, from which dependent claim 7 depends. The cited reference of Kunishima has a gate oxide film 5, a gate electrode, and an SiO2 film 23 and a BPSG film 25 sequentially deposited on top of a substrate. However, as discussed previously, Kunishima does not suggest a sidewall offset that extends along a surface of a gate oxide film on which the gate electrode is formed, as found in amended claim 6.

Applicant respectfully submits that the dependent claim 7, is patentable at least as depending upon a base claim shown above to be patentable. In view of the foregoing, applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 1-4, 6, 8-10, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng, is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claims 1-4, 6, 8-10, 21 and 23 are neither disclosed nor suggested by the cited reference, whether taken alone, or in any combination with well known art.

Claim 1 is summarized above. Claims 2-4 depend from claim 1. Claim 6 is summarized above. Claims 8-10, 21 and 23 depend from claim 6. The cited reference of Cheng is discussed above.

For reasons similar to those set forth elsewhere herein, applicant respectfully submits that independent claims 1 and 6 are neither disclosed nor suggested by Cheng, whether taken alone, or in any combination with other known references. Specifically, the suggested reference of Cheng neither describes nor suggests the combination of features of a "... *sidewall offset extending along a surface of a gate oxide film on which said gate electrode is formed* ...", as recited in the independent claims. Cheng has a sidewall 38, but nothing regarding the sidewall extending along the surface to limit the location of a part of the structure. Thus, the suggested reference does not even discuss the problem, and uses the prior art approach of masking the gate oxide 21 to provide an edge definition for the silicide process. Thus the independent claims 1 and 6, as amended herein, and thus the dependent claims based upon them, are non obvious over Cheng.

In view of the foregoing, applicant respectfully requests that this rejection be withdrawn.

The rejection of claims 5, 7, 11, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Kunishima, is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claims 5, 7, 11, 21 and 23 are neither disclosed nor suggested by the suggested combination of cited references, whether taken alone, or in any combination.

The features of Cheng and Kunishima have been discussed above. The features of the independent claims upon which dependent claims 5, 7, 11, 21 and 23 are based are discussed above.

Applicant respectfully submits that the cited reference of Kunishima adds nothing to the other cited reference of Cheng, as discussed above, in that Kunishima also neither discloses nor suggests a semiconductor device that includes a sidewall offset extending along a surface of a gate oxide film on which the gate electrode is formed, as set forth in applicant's amended independent claims, from which dependent claims depend. The addition of a silicide layer is seen as adding nothing to the disclosure of Cheng, which was shown above to not render the independent claims obvious.

In view of the above discussion, applicant respectfully requests that this rejection, as set forth in the Office Action, be reconsidered and withdrawn.

Based on the above, applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-951-6676.

Respectfully submitted,
HUTCHINS, WHEELER & DITTMAR

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Date

Donald W. Muirhead
Reg. No. 33,978

Patent Group
Hutchins, Wheeler & Dittmar
101 Federal Street
Boston, MA 02110

26339
PATENT TRADEMARK OFFICE